

Introduction to VLSI Design (CSE 464)

Syllabus

Fall 2008

Schedule

Lecture: TR 12:30-1:50
Office Hours: TR 10:00-11:30

Texts

- Weste & Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed, Addison Wesley, 2005.
- Jan M. Rabaey, *Digital Integrated Circuits*, Second Edition, Prentice-Hall, 2003
- Patterson & Hennessy, *Computer Organization & Design*, 2nd ed, Morgan Kaufmann, 1998.

CMOS VLSI Design is the primary text. However, the second book could be used as an alternative reference for the course. The course material to be covered can be found in both books. In this course you will learn about MOS VLSI technologies, CMOS digital circuits, Layout design, Simulation, Realization of digital subsystems-adders, memory, etc.

Electronic Communication

Class web page: BlackBoard@SU
Class email list: Through BlackBoard Announcement

Course Description

Our goal in this course is to study the process of implementing a digital system as a CMOS integrated circuit.

The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips. We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families. Afterwards, we will examine techniques for analysing and optimizing timing and power at the circuit level. We will study sequential elements—latches and flops—and clocking. This will be followed by an overview of datapath design: detection logic, shifters, comparators, adders, and multipliers. We will also study memories, specifically the workhorse 6-T SRAM cell as well as peripheral decode logic.

The course will conclude, subject to time availability, with a survey level treatment of various topics, including advanced circuit design techniques, clock tree design, functional verification, test, design-for-test, electrical effects, packaging, and future trends.

Grading

Labs: 30%
Final Project: 20%
Two Quiz Exams: 40%
Home Work Assignments: 10%

I will assign between 5 to 6 written homework, which will consist of questions from the book, and will be worth 10% of your grade. There will be two in-class midterms worth 40% of your grade. Four major lab design projects collectively worth 30% and a final project and presentation demo will make up the remainder of your grade. In order to pass the course you are required to receive at least half mark in each section.

Outline

Week	Material
Preliminaries	
Week 1 To Week 3	Introduction, history MOS transistor theory Lab 1 presentation
CMOS Circuit Characterization	
Week 3 To Week 5	DC & Transient Response Basic logic gate design Basic physical design Lab 2 presentation Logic effort Interconnect & Wire Engineering Lab 3 presentation <i>MIPS Project presentation</i> Midterm #1
CMOS circuit and logic design	
Week 5 To Week 10	Delay estimate SPICE Simulation Circuit families Lab 4 Presentation Sequential elements Adders Midterm #2
Datapath and Memories	
TBD	Clocking SRAMs ROMs, CAMs, PLAs Datapath-1 Datapath-2
Special Topics	
TBD	Test-1 Test-2 DSM effects Verification Verification Circuit pitfalls Low power Midterm 2 Clock trees, PLLs I/O Scaling-1 Scaling-2

Note: The course material might change during the semester depending on the progress of the class. All departmental, college and university regulation regarding class attendance, course drop, etc will be followed.